What is claimed is:

1. An integrated circuit to which IOs are separately provided and to which a write address and a read address are simultaneously input during one period of a clock signal, the integrated circuit comprising:

a plurality of memory blocks, each of the memory blocks having a plurality of sub-memory blocks;

data memory blocks corresponding to the memory blocks; and

a tag memory controlling unit, which writes data in the memory blocks or reads the data from the memory blocks in response to the write address or the read address;

wherein even though the simultaneously-input write address and read address are the same, access to the same sub-memory block is not simultaneously performed.

2. The integrated circuit of claim 1, wherein the sub-memory blocks are a set of memory cells for sharing a common word line or bit line.

3. The integrated circuit of claim 1, wherein in the sub-memory blocks, two or more word lines or bit lines cannot be simultaneously activated.

4. The integrated circuit of claim 1, wherein each of the data memory blocks has the same size as the size of one sub-memory block.

5. The integrated circuit of claim 1, wherein if each of the data memory block has the same size as the size of one sub-memory block, the data memory block may have the number of columns and rows different from the number of columns and rows of the sub-memory block.

6. The integrated circuit of claim 1, wherein the tag memory controlling unit has the same number of decoding addresses as the number of addresses for decoding the data memory blocks.

7. The integrated circuit of claim 6, wherein the tag memory controlling

unit has the number of columns and rows different from the number of columns and rows of each of the data memory blocks.

8. The integrated circuit of claim 1, wherein the tag memory controlling unit stores a data memory address indicating that data being currently stored in the data memory block is originally data corresponding to a sub-memory block, and valid determination information on determining whether data being currently stored in the data memory block is valid.

9. The integrated circuit of claim 8, wherein if the number of the sub-memory blocks is 2^N, each address of the tag memory controlling unit includes N+1 data bits, and N-bit of the N+1 data bits indicates a data memory address, and remaining 1-bit of the N+1 data bits indicates the valid determination information.

10. The integrated circuit of claim 1, wherein the data memory blocks have a direct mapping relation with the sub-memory blocks.

11. The integrated circuit f claim 1, wherein the data is input or output at a single data rate (SDR) or a double data rate (DDR).